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Total Number of Pages In This Submission

5

Application Number	10/040,473
Filing Date	January 9, 2002
First Named Inventor	Kia Silverbrook
Art Unit	2813
Examiner Name	Nema O Berezny
Attorney Docket Number	WSM09US

ENCLOSURES (Check all that apply)		
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT		
Firm or Individual name	Kia Silverbrook c/Silverbrook Research Pty. Ltd. 393 Darling Street, Balmain, NSW, 2041, Australia	
Signature		
Date	December 10, 2003	

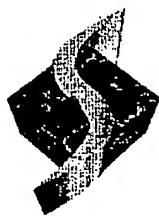
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Typed or printed name	Kia Silverbrook	
Signature		Date December 10, 2003

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Date **December 10, 2003**To: **Group Receptionist Art Unit 2813**Fax No.: **0011 1 703 872 9306**Subject: **United States Patent Application No. 10/040,473****Inventors/Assignors: Kia Silverbrook****Assignee: SILVERBROOK RESEARCH PTY LTD**Our Ref: **WSM09US**Total Number of Pages (including this) : **5****OFFICIAL**

Attached is a response to the Office Action dated October 15, 2003 of Examiner Nema O Berezny.

Regards

 Leonie News  
Silverbrook Research Pty Ltd

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T H E B U S I N E S S C O P Y N V E N T I O N

## In the United States Patent and Trademark Office

Serial Number: 10/040,473  
 Application Filed: January 9, 2002  
 Applicant: Kia Silverbrook  
 Application Title: LIGHT EMITTING SEMICONDUCTOR PACKAGE  
 Examiner/GAU: Nema O Berezny/2813

Dated December 10, 2003  
 At: Balmain, NSW  
 Docket No. WSM09US

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## REPLY

Commissioner for Patents  
 Washington, District of Columbia 20231

Dear Sir:

In response to the Office Action of October 15, 2003, please amend the above-identified application as follows:

The Applicant requests that the Examiner consider the remarks set forth below in response to the final Office Action mailed October 15, 2003. It is respectfully submitted that the claim rejections are incorrectly raised and the presently pending claims are not obvious in view of the cited prior art documents.

At pages 2-3 of the Office Action, the Examiner rejects claims 8-12 and 15 under 35 USC 103(a) as being unpatentable over Swirhun et al. in view of Cole. Reconsideration and withdrawal of this rejection is respectfully requested in light of the following arguments.

Swirhun et al. discloses an invention related to vertical cavity surface emitting lasers (VCSELs) and photodetectors. The Examiner construes lenses 136 and 138 of Fig 7b to disclose a hollow cap. It is clear that lenses 136 and 138 are standard lenses that can be formed over VCSEL 189, 92 and photodetector 62, 90, respectively, using materials which can be formed over chip 130 during the manufacturing of chip 130 or lenses that can be integrated with the surface of the plastic encapsulation formed by the package (col 10, lines 39-44). It is submitted that it is clear that lenses 136 or 138 do not disclose a first hollow cap as claimed in claim 8 of the present application.

A "first hollow cap" as defined in claim 8 requires "a central portion", "perimeter walls extending from the perimeter edge", "a first cavity", none of which are disclosed in Swirhun by lens 136 or 138. Lenses 136 and 138 are solid structures without a cavity, as illustrated in Fig 7b, such is the nature of a lens to allow refraction of electromagnetic radiation from the VCSEL. No cavity is disclosed or suggested in Swirhun.

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In micro-scale material processing to produce a refracting region within a hollow cap that is adapted to overly a light emitting device requires considerably more technological and manufacturing problems to be addressed and overcome than merely placing a solid lens over a light emitting device as is disclosed in Swirhun. Nowhere does Swirhun suggest or teach use of a first hollow cap to be bonded to the semi-conductor chip at the wafer stage prior to separation of the wafer into individual packages and where the first hollow cap includes a central portion and perimeter walls, with only the free edges of the perimeter walls bonded to the top surface to provide a cavity, and at least one region of the central portion transparent or translucent to the electromagnetic radiation. Although the at least one region of the central portion of the first hollow cap may be a lens, the Examiner has not considered all other features of a first hollow cap defined in claim 8 which distinguish claim 8 from Swirhun.

The skilled person reading the specification of Swirhun in its entirety is clearly only taught that the lens 136 is a solid feature. The Examiner's interpretation of the lens 136 in Fig 7b as being a hollow cap is respectfully submitted to be incorrect.

Neither does any disclosure in Cole teach or suggest use of a first hollow cap as defined in claim 8. The Examiner also relies on supposed disclosures in Cole concerning separation of the wafer into individual packages after a first hollow cap has been bonded to the semi-conductor chip at the wafer stage. It is respectfully submitted that Cole does not disclose or suggest such a feature. Referring to Figs 3 and 4 of Cole, package cover 130 is sealed to substrate 141, the ambient atmosphere is evacuated from cavity 134 and a vacuum-deposited plug 135 seals port 133. The wafer then contains multiple patterns, and the substrate contains a corresponding number of detector arrays. These can be sealed together and evacuated as a single unit. Block 480 then dices such a wafer into individual packages each containing a single array. (see sections [0027] and [0028]).

It is submitted that this discloses no more than conventional wafer cutting techniques well known in the prior art and to which the present invention is not directed. Cole does not disclose individual hollow caps bonded to a semiconductor chip which is then separated into individual packages. Cole discloses a complete wafer that is separated into individual packages. In Cole, each individual package containing a single array has not been provided with a protective or refractive hollow cap as defined in claim 8 of the present invention.

As is disclosed in the background art section of the present application (see page 1, line 9) semiconductor chips are normally packaged in a protective layer or layers to protect the chip and then chips are individually diced. It is submitted that this is precisely what is disclosed in Cole which does not disclose or suggest individual hollow caps bonded to the semiconductor chip prior to separation into individual packages with each individual package provided with a hollow cap. Cole merely discloses a block package cover 130 and subsequent cutting of the block unit.

The applicant submits that Swirhun and Cole are not relevant to the patentability of claim 8, and hence, dependent claims 9-15 are also neither anticipated or obvious in light of Swirhun and Cole, or in further view of Bloom that has been addressed and distinguished in the Applicant's earlier response.

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In view of the foregoing, it is respectfully requested that the Examiner reconsider and withdraw the rejections under 35 USC §103. The present application is believed to be in condition for allowance. Accordingly, the Applicant respectfully requests a Notice of Allowance of all the claims presently under examination.

Very respectfully,

Applicant:



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